

ABSTRACT OF THE DISCLOSURE

This invention has as its object to suppress an increase in circuit scale and to simplify a circuit structure by executing a filter process using a 5 plurality of arithmetic units each of which makes multiplication and addition.

To achieve this object, image data Y_{n+2} , Y_{n+3} , and Y_{n+4} to be processed are read out (S2901), and three lattice point data $d'n+1$, $S'n$, and $d'n-1$ are 10 respectively read out from sequences H_1 , H_2 , and H_3 corresponding to line buffers that store the lattice point data (S2903). $d'n+3 = Y_{n+3} + \alpha \cdot (Y_{n+2} + Y_{n+4})$ is computed (S2905), and $d'n+3$ is stored in the sequence H_1 (S2907). $S'n+2 + \beta \cdot (d'n+1 + d'n+3)$ is computed 15 (S2909), and $S'n+2$ is stored in the sequence H_2 (S2911). $d'n+1 = d'n+1 + \gamma \cdot (S'n+2 + S'n)$ is computed (S2913), and $d'n+1$ is stored in the sequence H_3 (S2915). $S_n = S'n + \delta \cdot (d'n-1 + d'n+1)$ is computed (S2917), and S_n and $d'n+1$ are output to the next processing stage (S2919).